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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,698	07/17/2003	Shinichi Watanabe	240429US2S	9303

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,698	WATANABE ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-16,19-21 and 23-25* is/are rejected.

7)☒ Claim(s) *10,11,17,18,22 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-26** are pending in this application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on applications filed in JAPAN, 2003-132703 on 05/12/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 07/17/2003 and made of record as Paper No. 091504. The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected for the following reason.

Figures 21-22 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-9, 12-16, 19-21 and 23-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (USP: 5,300,804) in view of Figure 21 of Applicant admitted prior art (AAPA).

Regarding claims **1-4**, Arai discloses in Fig. 2 and the corresponding texts as set forth in column 5, lines 35-55, each semiconductor device/each mask ROM device of the memory cell transistors comprises:

a semiconductor substrate (6);

a first trench/recess (5) formed in a surface of the semiconductor substrate and having a first side wall;

a first impurity diffusion area (13a) formed in the semiconductor substrate at a bottom of the first trench;

a second impurity diffusion area (13b) formed in the surface of the semiconductor substrate, having one end in contact with the first side wall, and having the same conductive type (N+) as that of the first impurity diffusion area; and

a first gate electrode (11) provided on the first side wall between the first impurity diffusion area and second impurity diffusion area with a gate insulating film (12) interposed therebetween.

Arai fails to teach a semiconductor device comprises:

a first lower electrode provided on the second impurity diffusion area;

a first ferroelectric film provided on the first lower electrode;

a first upper electrode provided on the first ferroelectric film;

a first interconnection layer provided above the first upper electrode;

a first contact plug electrically connecting the first interconnection layer and first impurity diffusion area together;

wherein the first upper electrode and the first interconnection layer are electrically connected together; and

wherein first contact plug partly provided in the first trench.

Figure 21 of AAPA and the corresponding texts as set forth in the Description of the Related Art teach that each semiconductor memory device of the memory cell transistors comprises:

a first lower electrode (111) provided on a second impurity diffusion area (103a);

a first ferroelectric film (112) provided on the first lower electrode;

a first upper electrode (113) provided on the first ferroelectric film;

a first interconnection layer (123) provided above the first upper electrode;

a first contact plug (123) electrically connecting the first interconnection layer and first impurity diffusion (103b) area together; and

wherein the first upper electrode and the first interconnection layer are electrically connected together.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a semiconductor memory device of the memory cell transistors comprising a first lower electrode, a first ferroelectric film, a first upper electrode, a first interconnection layer, a first contact plug electrically connecting the first interconnection layer

and first impurity diffusion area together and the first upper electrode and the first interconnection layer are electrically connected together, as taught by Figure 21 of AAPA into Arai's structure, and it is inhering the first contact plug is partly provided in the first trench, to arrive the claimed invention in order to provide a TC-parallel-unit series connection type ferroelectric memory of the memory cells.

Regarding claims **5-7**, Arai discloses in Fig. 2 the device further comprises:

a second trench/recess (5) formed in the surface of the semiconductor substrate apart from the first trench and having a second side wall located opposite to the first side wall with a part of the semiconductor substrate positioned therebetween, the second side wall contacts the other end of the second impurity diffusion area;

a third impurity diffusion area (13a) formed in the semiconductor substrate at a bottom of the second trench and having the same conductive type (N+) as that of the first impurity diffusion area; and

a second gate electrode (11) provided on the second side wall between the second impurity diffusion area and third impurity diffusion area with a gate insulating film (11) interposed therebetween.

Arai fails to teach the device further comprises:

a second ferroelectric film provided on the first lower electrode, the second ferroelectric film being apart from the first ferroelectric film;

a second upper electrode provided on the second ferroelectric film;

a second interconnection layer provided above the second upper electrode; and

a second contact plug electrically connecting the second interconnection layer and the third impurity diffusion area together; and

wherein the second upper electrode and the second interconnection layer are electrically connected together.

Figure 21 of AAPA teaches that each semiconductor memory device of the memory cell transistors further comprises:

a second ferroelectric film (112) provided on the first lower electrode (111), the second ferroelectric film being apart from the first ferroelectric film;

a second upper electrode (113) provided on the second ferroelectric film;

a second interconnection layer (123) provided above the second upper electrode; and

a second contact plug (124) electrically connecting the second interconnection layer and the third impurity diffusion area together; and

the second upper electrode and the second interconnection layer are electrically connected together.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a semiconductor memory device of the memory cell transistors comprising a second lower electrode, a second ferroelectric film, a second upper electrode, a second interconnection layer, a second contact plug electrically connecting the second interconnection layer and the third impurity diffusion area together and the second upper electrode and the second interconnection layer are electrically connected together, as taught by Figure 21 of AAPA into Arai's structure, and it is inhering the second contact plug is partly

provided in the second trench, to arrive the claimed invention in order to provide TC-parallel-unit series connection type ferroelectric memory cells.

Regarding claims **8-9**, Arai discloses in Fig. 2 the device further comprises:

a fourth impurity diffusion area (13b) formed the surface of the semiconductor substrate, having one end contacting the third side wall located opposite to the first side wall of the first trench, and having the same conductive type (N+) as that of the first impurity diffusion area; and

a third gate electrode (11) provided on the third side wall between the first impurity diffusion area and fourth impurity diffusion area with a gate insulating film (12) interposed therebetween.

Arai fails to teach the device further comprises:

a second lower electrode provided on the fourth impurity diffusion area;

a third ferroelectric film provided on the second lower electrode;

a third upper electrode provided on the third ferroelectric film; and

wherein the first and third upper electrodes and the first interconnection layer are electrically connected together.

Figure 21 of AAPA teaches that each semiconductor memory device of the memory cell transistors further comprises:

a second lower electrode (111) provided on the fourth impurity diffusion area;

a third ferroelectric film (112) provided on the second lower electrode;

a third upper electrode (113) provided on the third ferroelectric film; and

wherein the first and third upper electrodes and the first interconnection layer are electrically connected together.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a semiconductor memory device of the memory cell transistors comprising a second lower electrode, a third ferroelectric film, a third upper electrode, and the first and third upper electrodes and the first interconnection layer are electrically connected together, as taught by Figure 21 of AAPA into Arai's structure to arrive the claimed invention in order to provide TC-parallel-unit series connection type ferroelectric memory cells.

Regarding claims **12 and 14-16**, Arai discloses in Fig. 2 and the corresponding texts as set forth in column 5, lines 35-55, a semiconductor memory device/a mask ROM device having a plurality of memory cells connected in series, the memory cells each including a transistor (10a, 10b),

wherein each transistor comprises:

a first impurity diffusion area (13a) formed in a semiconductor substrate (6) at a bottom of one of plurality of trenches (5) formed in a surface of the semiconductor substrate;

a second impurity diffusion area (13b) formed in the surface of the semiconductor substrate between the trenches, having opposite ends contacting side walls of the trenches, and having the same conductive type (N+) as that the first impurity diffusion area; and

a gate electrode (11) provided on the side wall the trench between the first impurity diffusion area and the second impurity diffusion area with a gate insulating film (12) interposed therebetween.

Arai fails to teach a semiconductor memory device/a mask ROM device having capacitor and each capacitor comprises:

a lower electrode provided on the second impurity diffusion area;

a ferroelectric film provided on the lower electrode; and

an upper electrode provided on the ferroelectric film.

Figure 21 of AAPA and the corresponding texts as set forth in the Description of the Related Art teach that each capacitor comprises:

a lower electrode (111) provided on a second impurity diffusion area (103a);

a ferroelectric film (112) provided on the lower electrode; and

an upper electrode (113) provided on the ferroelectric film.

wherein the capacitors include first capacitors each electrically connected to the corresponding first transistor and second capacitors each electrically connected corresponding second transistor, and

the semiconductor memory device further comprises a plurality interconnection layers (123) each of which electrically connects the upper electrode of one of the first capacitor and the upper electrode of the corresponding second capacitor together, and a plurality of contact plugs (124) each of which electrically connects one of the interconnection layer and first impurity diffusion area together; and wherein each of the lower electrodes shared by the corresponding first transistors and the second transistor provided in the trench adjacent to the trench in which this first transistor is provided.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a capaciotr comprising a lower electrode, a ferroelectric film, an upper electrode, and wherein the capacitors include first capacitors each electrically connected to the corresponding first transistor and second capacitors each electrically connected corresponding second transistor, and the semiconductor memory device further comprises a plurality

interconnection layers each of which electrically connects the upper electrode of one of the first capacitor and the upper electrode of the corresponding second capacitor together, and a plurality of contact plugs each of which electrically connects one of the interconnection layer and first impurity diffusion area together, as taught by Figure 21 of AAPA into Arai's structure in order to provide a TC-parallel-unit series connection type ferroelectric memory and it is inhering each of the contact plug is partly provided in the corresponding trench, and each of the lower electrodes is shared by the corresponding first transistors and the second transistor provided in the trench adjacent to the trench in which this first transistor is provided.

Regarding claim **13**, Arai discloses in Fig. 2 the device wherein the transistors include first transistors each provided along a first side wall of a corresponding one of the plurality of trenches and second transistors each provided along a second side wall opposite the first side wall.

Regarding claim **19**, Arai discloses in Fig. 2 and the corresponding texts as set forth in column 5, lines 35-55, a method of manufacturing a semiconductor memory device/a mask ROM device comprises:

forming a trench (5) in a surface a semiconductor substrate (6);

forming a first impurity diffusion area (13a) in the semiconductor substrate at a bottom of the trench;

forming a gate insulating film (12) on a side wall and the bottom of the trench;

forming a gate electrode (11) on the gate insulating film; and

forming a second impurity diffusion area (13b) in the surface of the semiconductor substrate, the second impurity diffusion area having one end contacting the side wall of the

trench, the second impurity diffusion area having the same conductive type (N+) as that of the first impurity diffusion area.

Arai fails to teach a method of manufacturing a semiconductor memory device comprises:

forming a lower electrode on the second impurity diffusion area;

forming a ferroelectric film on the lower electrode;

forming an upper electrode on the ferroelectric film;

forming a contact plug electrically connected to the first impurity diffusion area; and

forming an interconnection layer above the upper electrode, the interconnection layer being electrically connected to the contact plug.

Figure 21 of AAPA and the corresponding texts as set forth in the Description of the Related Art teach that a method of manufacturing a semiconductor memory device comprises:

forming a lower electrode (111) on a second impurity diffusion area (103a);

forming a ferroelectric film (112) on the lower electrode;

forming an upper electrode (113) on the ferroelectric film;

forming a contact plug (124) electrically connected to a first impurity diffusion area (103b); and

forming an interconnection layer (123) above the upper electrode, the interconnection layer being electrically connected to the contact plug.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a semiconductor memory device of the memory cell transistors comprising of forming a lower electrode, a ferroelectric film, an upper electrode, a contact plug

electrically connecting the first impurity diffusion area and an interconnection layer are electrically connected to the contact plug, as taught by Figure 21 of AAPA into Arai's structure, and it is inhering the first contact plug is partly provided in the first trench, to arrive the claimed invention in order to provide a TC-parallel-unit series connection type ferroelectric memory of the memory cells.

Regarding claims **20 and 24**, Arai discloses in Figs. 2 and 7-8, the method wherein forming the gate electrode comprises burying a material film (12a) for the gate electrode in the trench(es); and patterning the material film so that a part of the material film trench(es) remains.

Regarding claims **21 and 25**, Arai discloses in Figs. 2 and 7-8, the method wherein forming the gate electrode comprises depositing a material film (12a) for the gate electrode on the side wall and bottom of the trench(es), the material film having a larger film thickness than the gate electrode; and removing a part of the material film on the bottom of the trench(es).

Regarding claim **23**, Arai discloses in Fig. 2 and the corresponding texts as set forth in column 5, lines 35-55, a method of manufacturing a semiconductor memory device/a mask ROM device having a plurality of memory cells connected in series, the memory cells each including a transistor, the method comprises:

forming a plurality of trenches (5) in a surface of a semiconductor substrate (6), the trenches being apart from one another;

forming first impurity diffusion areas (13a) in the semiconductor substrate at a bottom of each of the trenches;

forming gate insulating films (12) on side walls and a bottom of each of the trenches;

forming gate electrodes (11) on each of the gate insulating films;

forming second impurity diffusion areas (13b) in the surface of the semiconductor substrate between the adjacent trenches, the second impurity diffusion areas each having opposite ends contacting the side walls of the trenches and having the same conductive type (N+) as that of the first impurity diffusion area.

Arai fails to teach a method of manufacturing a semiconductor memory device comprises:

forming lower electrodes on each of the second impurity diffusion areas;

forming ferroelectric films on each of the respective lower electrodes, the ferroelectric films being apart from one another;

forming upper electrodes on each of the respective ferroelectric films;

forming contact plugs electrically connected to each of the first impurity diffusion areas; and

forming interconnection layers above the respective upper electrodes, the interconnection layers each being electrically connected to each of the contact plugs.

Figure 21 of AAPA and the corresponding texts as set forth in the Description of the Related Art teach that a method of manufacturing a semiconductor memory device comprises:

forming lower electrodes (111) on each of the second impurity diffusion areas;

forming ferroelectric films (112) on each of the respective lower electrodes, the ferroelectric films being apart from one another;

forming upper electrodes (113) on each of the respective ferroelectric films;

forming contact plugs (124) electrically connected to each of the first impurity diffusion areas; and

forming interconnection layers (123) above the respective upper electrodes, the interconnection layers each being electrically connected to each of the contact plugs.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a semiconductor memory device having a plurality of the memory cells comprising of forming lower electrodes, ferroelectric films, upper electrodes, contact plugs electrically connecting the impurity diffusion areas and interconnection layers are electrically connected to the contact plugs, as taught by Figure 21 of AAPA into Arai's structure to arrive the claimed invention in order to provide TC-parallel-unit series connection type ferroelectric memory cells.

Allowable Subject Matter

Claims **10-11, 17-18, 22 and 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Arai and Figure 21 of AAPA, whether taken alone or in combination, fail to teach the claimed limitation the device further comprises a first insulating film covering the first gate electrode; and a second insulating film which is buried in the first trench and different from the first insulating film as recited in claim **10**; the device further comprises a plurality of first insulating films each of which covers a corresponding one of the plurality of gate electrodes; and a plurality of second insulating films each of which is buried in a corresponding one of the plurality of trenches, the second insulating films different from the first insulating films as recited in claim **17**; the method

further comprises forming a first insulating film on the gate electrode, the first insulating film being composed of a material different from that of the gate electrode; and burying a second insulating film in the trench, the second insulating film being different from the first insulating film as recited in claim **22**; and the method further comprises forming first insulating films on the respective gate electrodes, the first insulating films being each composed of a material different from that of the gate electrodes; and burying a second insulating film in each of the trenches, the second insulating film being different from the first insulating film as recited in claim **26**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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09/15/04

Andy Huynh

Patent Examiner